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Arai et al.

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(54) **NORMALLY-OFF POWER JFET AND MANUFACTURING METHOD THEREOF**

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(58) **Field of Classification Search**
None
See application file for complete search history.

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(57) **ABSTRACT**

In general, in a semiconductor active element such as a normally-off JFET based on SiC in which an impurity diffusion speed is significantly lower than in silicon, gate regions are formed through ion implantation into the side walls of trenches formed in source regions. However, to ensure the performance of the JFET, it is necessary to control the area between the gate regions thereof with high precision. Besides, there is such a problem that, since a heavily doped PN junction is formed by forming the gate regions in the source regions, an increase in junction current cannot be avoided. The present invention provides a normally-off
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